Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte VICTOR M. DACOSTA, and ALAN G. LEWIS

Appeal No. 1998-3044
Application 08/458,539[1]

ON BRIEF

Before SCHAFER, Senior Administrative Patent Judge, and LEE and MEDLEY, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's rejection of appellants' claims 1-12. No claim has been allowed. The real party in interest is Xerox Corporation.

References relied on by the Examiner

Hatada et al. (Hatada)	4,766,426	Aug. 23, 1988
Duwaer	4,922,240	May 01, 1990
Fukuda	5,162,786	Nov. 10, 1992
Ishimaru	5,532,718	July 02, 1996

[1] Application for patent filed June 02, 1995.

The Rejection on Appeal

Claims 1, 2, 6 and 7 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over Duwaer.

Claims 3, 4, and 10-12 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over Duwaer and Hatada.

Claim 5 stands finally rejected under 35 U.S.C. § 103 as being unpatentable over Duwaer and Ishimaru.

Claims 8 and 9 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over Duwaer and Fukuda.

The Invention

The claimed invention is directed to a device including digital-to-analog driving circuitry and multiplexer circuitry driven by the driving circuitry. The number of connecting data lines between the output of the driving circuitry and the input of the multiplexer circuitry is not less than 32. Claims 1, 10 and 12 are the only independent claims. Representative claim 1 is reproduced below:

> 1. A product comprising:
>
> a first substrate with a surface at which circuitry can be formed; and
>
> array circuitry formed at the surface of the first substrate, the array circuitry comprising:

a set of N data lines, where N is an integer greater than 32; each of the N data lines extending across the surface of the first substrate; each of the N data lines having a drive input lead in a multiplexer region of the surface of the first substrate; and

for each of the N data lines, M units of cell circuitry, each connected for receiving signals from the data line, where M is an integer greater than zero;

multiplexer circuitry formed in the multiplexer region of the surface of the first substrate; the multiplexer circuitry being connected to the drive input lead of each of the N data lines; the multiplexer circuitry comprising:

for each of the N data lines, a drive output lead connected for providing multiplexed signals to the data line’s drive input lead;

P analog input leads for receiving input analog drive signals, where P is an integer less than N but not less than 32; and

Q multiplexer control leads for receiving multiplexer control signals, where Q is an integar not less than N/P and less than N;

the multiplexer circuitry responding to the input analog drive signals and the multiplexer control signals by providing the multiplexed signals; and

one or more integrated circuit structures attached to the first substrate; the integrated circuit structures together comprising:

> R single crystal substrates, where R is an integer greater than zero; each single crystal substrate having a surface at which circuitry can be formed; and
>
> at the surface of each of the R single crystal substrates, digital-to-analog circuitry, the digital-to-analog circuitry on each substrate's surface having digital input leads and at least S analog output leads, where S is an integer not less than 32; the digital-to analog circuitry providing, on each analog output lead, an analog drive signal with an amplitude that varies with a value indicated by a digital drive signal received from the digital input leads; the R single crystal substrates together having T analog output leads, where T is an integer not less than P; each of the P analog input leads of the multiplexer circuitry being paired with and connected to one of the T analog output leads so that the R single crystal substrates together provide the input analog drive signals.

Opinion

The rejection of claims 1-12 is reversed.

A reversal of any rejection on appeal should not be construed as an affirmative indication that the appellants' claims are patentable over prior art. We address only the sufficiency of the findings and rationale as set forth by the examiner and on which the examiner's rejection is based.

According to the appellants, two problems tug at opposite ends of trying to produce an efficient driver for active

matrix liquid crystal displays. First, the appellants state (Br. at 4):

> In order to reduce the number of DACs or video amplifiers required, and hence lower system cost, the number of input lines to the DACs or video amplifiers can be reduced. The problem with doing this is that the width of the integrated multiplexers, required to deliver data on a small number of input lines to a much larger number of display data lines, must be increased. That is, each input line must serve more display data lines. All the data lines must be charged to the required data voltage within each horizontal line time. Thus, if fewer input lines are used (i.e., more display data lines per input line) the time available to charge each individual data line is reduced. The charging must take place through at least one polysilicon TFT. These devices have significantly lower channel conductance than conventional single crystal transistors, and thus the short charging time tends to degrade the accuracy with which the data lines are charged. The final voltages on the data lines at the end of each line time are transferred into the addressed row of pixels, and thus a lower precision of the data line voltage is reflected directly in less accurate pixel voltages. This degrades the ability of the display to render gray scales accurately, and reduces image quality.
>
> In order to maintain high image quality, the number of input lines can be increased. However, for each additional input line, an additional DAC or video amplifier is required, along with its associated support circuitry, and the cost and complexity of the external drive system goes up significantly.

The appellants explain that their invention solves the competing problems by providing a large number of data input lines without leading to a difficult packaging problem or a costly and complex external drive system requiring additional high voltage DACs or video amplifiers. (Br. at 5-6). This is done by providing the large number of input lines by coupling the active matrix liquid crystal display to "a single crystal driver chip" of the type commonly used to drive amorphous silicon TFT AMLCDs [active matrix liquid crystal displays]. (Br. at 5).

The appellants further state (Br. at 5-6):

> An example of such a driver chip is the Vivid VS1184, although others are available. These chips accept low voltage (3.3v or 5v) digital data through a bus only one or two pixels wide, and output analog data of the required amplitude in parallel. The VS1184, for example, provides 384 outputs. . . . Since there are now many input leads, the multiplexer width is narrow (i.e., the number of array data lines associated with each input lead is small) and the charging time available for each data line is long. Thus, each data line can be charged more precisely, and the voltage signals ultimately delivered to the pixels and AMLCD cells are more accurate, allowing accurate rendition of gray levels and high image fidelity.
>
> . . . . The data input is via the low voltage digital bus of the driver IC, and the control signals for this device are similarly low voltage and easy to generate. The only high voltage signals

> are the simple clock and (perhaps) enable signals required for the integrated scan circuits. **The need for additional high voltage DACs or video amplifiers is eliminated**. (Emphasis added.)

The statements of the appellants, while logical and convincing on its face, are not commensurate in scope with what the appellants have claimed. None of the claims recite the specially structured single chip driver circuit of the type discussed in the above-quoted text, which eliminates the need for high voltage DACs or video amplifiers. All of the claims do require the presence of digital-to-analog circuitry on single crystal substrates, but that recitation is broad enough to cover an integration of multiple and complex DACs and video amplifiers on a single chip, something the appellants seek to eliminate. The breadth of the claims cover the case where multiple high voltage DACs or video amplifiers are used but just all integrated on a single chip.

The examiner is correct that if the prior art teaches use of at least 32 data input lines, with use of multiple high voltage DAC's or video amplifiers, then simply integrating those components on a single chip would have been obvious to one with ordinary skill in the art, citing In re Larson, 144

USPQ 347 (CCPA 1965) and In re Lockart, 90 USPQ 214 (CCPA 1951).

The appellants argue that Duwaer does not disclose or suggest using at least 32 data input lines because the thrust of the Duwaer invention is aimed at reducing the number of data input lines and because the specifically disclosed example uses only 20 data input lines. The argument overlooks that a reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect, EWP Corp. v. Reliance Universal Inc., 755 F.2d 898, 907, 225 USPQ 20, 25 (Fed. Cir.), cert. denied, 474 U.S. 843 (1985), and that a reference must be evaluated for all its teachings and is not limited to its specific embodiments. In re Bode, 550 F.2d 656, 661, 193 USPQ 12, 17 (CCPA 1977); In re Snow, 471 F.2d 1400, 1403, 176 USPQ 328, 329 (CCPA 1973).

It is true that Duwaer's invention is directed to or aimed at reducing the number of data input lines. But that means it is cognizant of the performance characteristics of a device having many data input lines and seeks to improve them. The appellants do not point to any portion of Duwaer which

indicates that a count of data input lines in excess of 32 will render the device inoperable. Rather, a reasonable reading of Duwaer would simply reveal that there are advantages for having fewer data input lines. Indeed, as the examiner has indicated (Answer at 6), Duwaer in column 2, lines 11-17 and column 6, lines 23-35, indicates that a greater number of data input lines may be used but would increase the substrate area required and thus the cost.

Nonetheless, the appellants need to demonstrate only one winning argument to have the rejection on appeal reversed, and they have.

The appellants refute that a "sample and hold circuit" is a digital-to-analog converter as is required by all of the claims on appeal. The examiner, when faced with that challenge, has not produced any evidence that a sample and hold circuit is a digital-to-analog converter. The appellants also point out that even if Duwaer's sample and hold circuits are replaced with digital-to-analog converters, the resulting combination would not function, because Duwaer's sample and hold circuits receive analog signals as inputs. The examiner, in response, has not produced any evidence that Duwaer's

sample and hold circuits actually receive incoming digital signals as input. Instead, the examiner states (Answer at 7):

> However, even arguendo that the input signal in the device of Duwaer is analog, it would have been obvious for one ordinary skill in the art at the time the invention was made to use a DAC for converting the incoming digital signal into analog signal so that the driving circuitry would have been able to apply the digital signal to the display elements having analog operation.

The above-quoted statement is self-contradictory. If it is assumed that Duwaer's input signal is analog, as is stated in the first part of the sentence, then there is no incoming digital signal for the examiner to properly refer to in the second part of the same sentence. The examiner further states (Answer 7):

> In addition, it should be noted that applicant also admitted that a DAC has been used in a conventional LCD display device for converting the digital input signal into analog signal (see page 5 in the specification).

That admission, even if assumed to have been made, does not help the examiner in an environment where the examiner has not specifically identified digital input signals for conversion. None of the other references, Hatada, Ishimaru, and Fukuda, as relied on and applied by the examiner, cures the deficiency.

We decline to attempt a salvage of the examiner's deficient rejection by either (1) digging into Duwaer at a level beyond that addressed by the examiner, or (2) buttressing the examiner's inadequate positions with additional rationale not expressed by the examiner. It is not our role to conduct examination in the first instance, nor is it fair to the appellants to have a rejection affirmed based on a position or rationale not explained by the examiner. A poorly articulated and/or inadequately formulated rejection has its consequences, i.e., the applicant for patent has not been shown that he or she is not entitled to a patent. We decline to ponder or to speculate as to whether another rationale, another critical finding, or clearer explanations could have been made by the examiner, which would have cured the deficiencies in the rejections on appeal. It suffices to say only that the rejections as advanced and presented by the examiner in this appeal cannot be sustained.

A rejection that is 99% adequate is still 100% inadequate. An almost good rejection is not a good rejection.

Conclusion

The rejection of claims 1, 2, 6 and 7 under 35 U.S.C. § 103 as being unpatentable over Duwaer is reversed.

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REVERSED

RICHARD E. SCHAFER Administrative Patent Judge	)
JAMESON LEE Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
SALLY C. MEDLEY Administrative Patent Judge	)

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